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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,693	12/11/2003	Wayne A. Britson	ROC920030248US1	8659
30206 7590 03/16/2007 IBM CORPORATION ROCHESTER IP LAW DEPT. 917 3605 HIGHWAY 52 NORTH ROCHESTER, MN 55901-7829			EXAMINER RIZK, SAMIR WADIE	
			ART UNIT 2133	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE			MAIL DATE	DELIVERY MODE
3 MONTHS			03/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/733,693

Applicant(s)

BRITSON ET AL.

Examiner

Sam Rizk

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.


GUY LAMARRE
PRIMARY EXAMINER

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 12/19/2006
- Claims 1-20 have been submitted for examination
- Claims 1-20 have been rejected

Specification

1. In view of the applicant-amended title filed on 12/19/2007, all objections to the specification are withdrawn.

Drawings Objections

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore:
 - The "plurality of input lines" as in claims 1 and 10 must be shown as **two separate lines**. However, these "plurality of input lines" in FIG. 1, reference characters (116) and (118) in FIG. 1 are shown connected, or the feature(s) must be canceled from the claims 1 and 10. No new matter should be entered.
 - Same objection are applied for FIG. 3, reference characters (312), (314), (316), (318), (320) and (322).
3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show description of each of the following reference characters (306), (308), (310), (338), (340) and (346) as described in the specification. Any structural detail that

is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Response to Arguments

4. Applicant's arguments with respect to claims 1 and 10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 6, 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Watari US patent no. 4894708 (Hereinafter Watari).

6. In reference to claim 1, Watari teaches:

- employing one of a plurality of input lines to receive a test signal for a processor;

(Note: FIG. 2, reference characters (1), (1,1a), (8), (8a) and col. 3, lines (4-14) in Watari)

- employing one of a plurality of output lines to send a test result from the processor; and

(Note: FIG. 2, reference characters (1), (1,1a), (8), (8a) and col. 3, lines (4-14) in Watari)

- if the test result is unsuccessful, performing at least one of:

(Note: col. 3, lines (23-26) in Watari)

- employing a remaining one of the plurality of input lines to receive the test signal for the processor; and

(Note; col. 3, lines (23-42) in Watari)

- employing a remaining one of the plurality of output lines to send the test result from the processor.

(Note; col. 3, lines (23-42) in Watari)

7. In regard to claim 2, Watari teaches:

- applying the test signal to each of the plurality of input lines;

(Note: FIG. 2, any of reference characters ((1), (1,1a), (8), (8a) in Watari)

- selecting one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

receiving the test signal for the processor from the selected input line.

(Note: FIG. 2, reference character (8a) in Watari)

8. In regard to claim 3, Watari teaches:

- applying the test result to each of the plurality of output lines;

(Note: FIG. 2, any of reference characters ((1), (1,1a), (8), (8a) in Watari)

- selecting one of the plurality of output lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- sending the test result from the processor using the selected output line.

(Note: FIG. 2, reference character (8a) in Watari)

9. In regard to claim 4, Watari teaches:

- selecting a remaining one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of input lines to receive the test signal.

(Note: FIG. 2, reference character (8a) in Watari)

10. In regard to claim 6, Watari teaches:

- selecting a remaining one of the plurality of output lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 2, reference character (8a) in Watari)

11. In regard to claim 8, Watari teaches:

- employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:

- selecting a remaining one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of input lines to receive the test signal; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing a remaining one of the plurality of output lines to send the test result from the processor includes:

- selecting a remaining one of the plurality of output lines; and

(Note: FIG. 2, reference character (8a) in Watari)

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- employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 2, reference character (8a) in Watari)

12. Claim 10 is rejected for the same reasons as per claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
13. Claims 5, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watari as applied to claim 4 above, and further in view of Bombal et al. US patent no. 6141782 (Hereinafter Bombal).
14. In regard to claim 5, Watari teaches substantially all the limitations in claim 4. However, Watari does not teach:
- modifying a first select signal; and

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Bombal in an analogous art that teaches pseudo-scan using hardware accessible

IC structures teaches:

- modifying a first select signal; and

(Note: FIG. 8, third block in Bombal) and

Watari teaches:

- selecting a remaining one of the plurality of input lines based on the modified first select signal.

(Note: FIG. 2, reference character (8a) in Watari)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Watari that teaches parallel I/O testing of an IC with the teaching of Bombal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need for an efficient IC fault coverage.;

15. In regard to claim 7, Bombal teaches:

- modifying a second select signal; and

(Note: FIG. 8, third block in Bombal) and

Watari teaches:

- selecting a remaining one of the plurality of output lines based on the modified second select signal.

(Note: FIG. 2, reference character (8a) in Watari)

16. In regard to claim 9, Bombal teaches:

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- selecting a remaining one of the plurality of input lines includes:
- modifying a first select signal; and

(Note: FIG. 8, third block in Bombal) and

- selecting a remaining one of the plurality of input lines based on the modified first select signal; and

(Note: FIG. 2, reference character (8a) in Watari)

- modifying a second select signal; and

(Note: FIG. 8, third block in Bombal) and

- selecting a remaining one of the plurality of output lines based on the modified second select signal.

(Note: FIG. 2, reference character (7a) in Watari)

17. Claims 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watari as applied to claim 4 above, and further in view of Evans US publication no. 2003/0208713 (Hereinafter Evans).

18. In regard to claim 11, Watari substantially teaches all the limitations in claim 10. However, Watari does not teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and
- further comprising a first multiplexer coupled to the plurality of input lines and the processor, and adapted to:
 - select one of the plurality of input lines; and
 - receive the test signal for the processor on the selected input line.

Evans in an analogous art that teaches a test head performs at-speed testing of high serial pin count devices teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and
- further comprising a first multiplexer coupled to the plurality of input lines and the processor, and adapted to:

(Note: FIG. 10, reference character (312A) in Evans)

- select one of the plurality of input lines; and

(Note: FIG. 10, reference character (114C) in Evans)

- receive the test signal for the processor on the selected input line.

(Note: FIG. 10, reference character (810) in Evans)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Watari that teaches parallel I/O testing of an IC with the teaching of Evans.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to minimize IC line failures.

19. In regard to claim 12, Watari teaches:

- select a remaining one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employ the selected remaining one of the plurality of input lines to receive the test signal.

(Note: FIG. 2, reference character (8a) in Watari)

20. In regard to claim 13, Evans teaches:

- The apparatus of claim 11 further comprising a third multiplexer coupled to the connector interface and first multiplexer, and adapted to modify a first select signal, the first select signal corresponding to the first multiplexer; and

(Note: FIG. 8, third block in Bombal) and FIG. 10, reference character (308) in Evans)

- wherein the first multiplexer is further adapted to select a remaining one of the plurality of input lines based on the modified first select signal.

(Note: FIG. 10, reference character (312A) in Evans)

21. In regard to claim 14, Evans teaches:

- The apparatus of claim 10 wherein the processor is adapted to apply the test result to each of the plurality of output lines; and
- further comprising a second multiplexer coupled to the plurality of output lines and the connector interface, and adapted to:

(Note: FIG. 10, reference character (308) in Evans)

- select one of the plurality of output lines; and
- send the test result from the processor using the selected output line.

(Note: FIG. 10, reference character (114C) in Evans)

22. Claim 15 is rejected for the same reasons as per claim 12.

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23. Claim 16 is rejected for the same reasons as per claim 13.

24. In regard to claim 17, Evans teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and further comprising a first multiplexer coupled to the plurality of input lines and the processor, the first multiplexer adapted to:

(Note: FIG. 10, reference character (312A) in Evans)

- select one of the plurality of input lines; and
- receive the test signal for the processor from the selected input line;

(Note: FIG. 10, reference character (810) in Evans)

- wherein the processor is further adapted to apply the test result to each of the plurality of output lines; and
- further comprising a second multiplexer coupled to the plurality of output lines and the connector interface, the second multiplexer adapted to:

(Note: FIG. 10, reference character (308) in Evans)

- select one of the plurality of output lines; and
- send the test result from the processor using the selected output line.

(Note: FIG. 10, reference character (308) in Evans)

25. Claim 18 is rejected for the same reasons as per claim 15

26. Claim 19 is rejected for the same reasons as per claim 9.

27. In regard to claim 20, Evans teaches:

- The apparatus of claim i0 wherein the connector interface is adapted to couple to a service processor.

(Note: FIG. 1A, reference character (102) in Evans)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

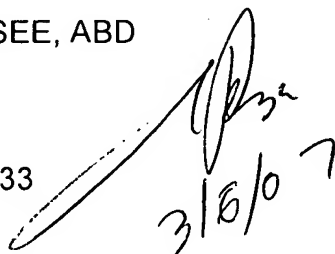
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

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Sam Rizk, MSEE, ABD

Examiner

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